Delay Depreciation and Power efficient Carry Look Ahead Adder using CMOS

T. Archana*, K. Arunkumar, A. Hema Malini

Department of Electronics and Communication Engineering, Saveetha Engineering College, Chennai, India.

*Corresponding author: E-Mail: archana@saveetha.ac.in

ABSTRACT

Adder is the major component in all data path unit. In this paper, designing of fast adder has been done by carry look ahead adder instead of ripple carry adder. Since the RCA has worst propagation delay of carry bit. Power and area remain the main constraint in designing of VLSI circuits. By reducing the number of MOS and FET, the power usage of MOS circuit would positively be reduced. Typical CLAs would use huge quantity of power which should be reduced. In this paper, we execute an 8-bit CLA with smaller size and dropping down the power consumption, by improving the basic working component of the circuit. By using Cadence Virtuoso tool each parameter have been calculated. This tool is used to display the waveform and analysis the RF, mixed and analog signal to realize and decide their effects on performance of the circuit.

KEY WORDS: CLA, RCA, MOS.

1. INTRODUCTION

VLSI technology: The Electronics industry revolution is created by discovery of transistor by William B. Shockley, Walter H. Brattain and John Bardeen of Bell Telephone Laboratories. This leads to the growth of Integrated circuit technology. Jack Kilby invented the first IC at Texas Instruments in 1960. In VLSI technology MOS transistor design process plays important role. The MOS transistor design based on PMOS, NMOS, CMOS and Bi-CMOS devices.

By sandwiching many layers of conducting insulating materials the Metal oxide semiconductor is formed. CMOS consists of two type of metal oxide semiconductor transistor namely n-type and p-type material. It is based on the operation of electric fields so the device is called Metal Oxide Field Effect Transistors.

All transistors has a conducting gate, silicon dioxide (SiO_2) which is insulating layer (known as glass) and the substrate or body or bulk which silicon wafer. An NMOS semiconductor consists of p-type and n-type material in which p-type contact led connected as body and n-type contact led connected as drain. The substrate of NMOS is grounded. A PMOS semiconductor consists of n-type material as body and p-type material as drain and source. The substrate of PMOS should be connected to V_{dd}.

In Complementary metal oxide is combination of both NMOS & PMOS. In NMOS semiconductor the majority charge carrier is electrons and it flows from source to drain in conducting path. So, NMOS is in ON state. In PMOS semiconductor the majority charge carrier is holes and flows from source to drain in conducting path. So, PMOS is in ON state. When PMOS is on and it is connected to V_{dd} which gives output of a logic '1' in digital circuits. Likewise, NMOS is on and it is connected to Gnd which gives output of a logic '0'.

The source and drain of the MOSFET has been controlled by gate of the MOSFET. When input to gate terminal is applied as '1', NMOS transistor gets ON and it is connected to ground. When input to gate terminal is applied as '0', PMOS transistor gets ON and it is connected to V_{dd}.

Literature Survey: High speed adders are designed using 130nm CMOS process and are being evaluated for their performance at lower technologies. The comparison of RCA and CLA made through the delay, power dissipation and area.

The 28 transistor static CMOS full adder which is taken as a base cell is used. By cascading n-bit full adders ripple carry adders can be constructed. In CLA operation, the carry from previous stage is forwarded to next stage. Thus the output ripples through the subsequent stages and forms the output carry of the MSB adder. Since the output traverses the longest critical path, this adder shows the worst case delay.

The fastest adder discussed under this category is carry look ahead adder (CLA). Advance calculation of carry signals avoid the delay caused in the ripple carry adders. The working of CLA is based upon the generation of carry out if and only if inputs A=B=1 or when A/B = carry in = 1. Figure.1, shows the schematic of 4-bit CLA. For greater than 4-bits the CLA becomes complex is the designing becomes complicated.
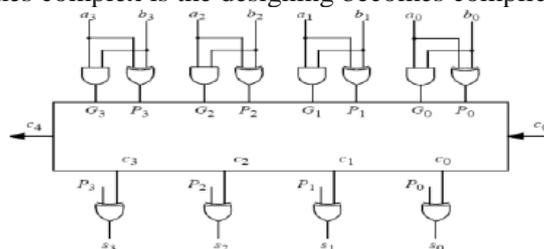

Figure.1. Schematic of 4-bit CLA

Performance Analysis: Four bit high-speed adders RCA, CLA have been designed in a standard 130 nm CMOS technology using Mentor Graphics tools. Average Power dissipation of all the high-speed adders is measured for a supply voltage V_{dd} =1V. All the adders have been designed using the conventional 28 transistor static full adder cell. The analysis has been done by simulation result that CLA consumes power but it is about 50% faster as compared to the ripple carry adders. Thus, CMOS four-bit RCA, CLA circuits have been designed and implemented in 130nm CMOS technology and compared for power, delay and area. All the circuits have been simulated at supply voltage of 1V. It is shown that the delay is minimum for the CLA.

Here Carry look ahead adder is designed with new methodology. By using Cadence gate delay simulation we can achieve faster speed in proposed CLA. The Proposed CLA uses NAND gate which swap the AND and OR gate used in conventional CLA which in turn decreases the price of conventional CLA and increases the speed.

The conventional CLA has been modified with slight changes as modified carry look ahead adder (referred as MCLA). MCLA has basic arithmetic adder circuit.

Proposed look ahead adder and arithmetic adder is constructed using NAND gate. To improve the speed of CLA a new method also proposed in this paper. To speed up the circuit operation the recursive circuit is used. Here CLA and MCLA used as recursive circuits. The proposed design will have improvement in both cost and efficiency. The proposed design of the 4-bit CLA is shown in Figure.2.
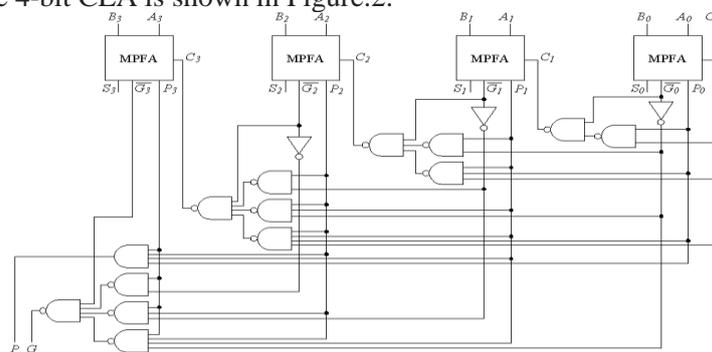

Figure.2. Proposed design of 4-bit MCLA

To progress the efficiency of CLA, fundamental module like Ex-OR and full adder are required for suitable application. The major goal of this paper is to decrease the power utilization and area occupied by arithmetic adder. All parameter has been calculated by analysis made by Cadence tool which uses the 45nm technology.

The implementation of CLAs reduces the time required to produce propagate and generate carry bit. But, reduction of power consumption becomes important factor in all ICs. The low power and area requirement can be achieved by designing CLA. To achieve this, before designing 8 bit CLA, have implement 4 bit CLA. In this proposed system to get 8-bit CLA, two 4-bit CLAs are cascaded. So that we can achieve power consumption in minimal amount and reduced area. It is much easier to construct 8-bit CLA by cascading two 4-bit CLAs than design of complex 8-bit CLA.

In this paper, the 4-bit CLA has been designed with 29% of reduced power consumption. With this reduction in power consumption, 8-bit CLA has been designed. The design of a 4-bit CLA is shown in Figure.3.
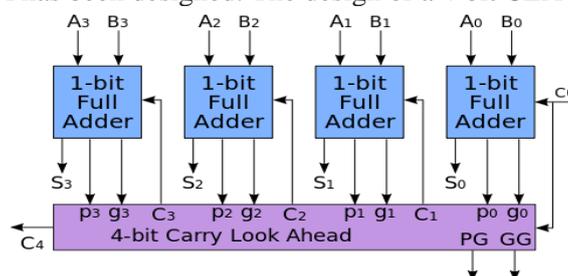
Figure.3. Block diagram of 4-bit CLA

By decreasing the power consumption the rate of bit accessed in CLA is increased and threshold level of MOS has been decreased to 3.35ns. Obviously the reduction in power of 4-bit CLA reduce the 8-bit CLA power.

2. PROPOSED SYSTEM AND DESIGN ANALYSIS

The most common and widely used arithmetic function is addition. The adder circuit is the basic building block of many digital systems like multipliers, processors to implement various algorithms. The digital circuits or systems are desired to have high speed and should be able to operate at high frequencies.

The number stages in adder circuit decides propagation delay of RCA. The more of stages adds the delay of carry bit from LSB to MSB position. The problem in RCA adder is trounced by (CLA) in adder circuits.

The main aim of our project is to design an 8-bit CLA with minimal power consumption and less delay. With the help of basic logic gate 8-bit CLA has been design. The circuit design and the simulation of the CLA is held by Cadence Virtuoso tool which uses 180nm technology. Taking into account the circuit complexity, it would be easier to design an 8-bit CLA using the cascaded configuration. In this paper, by using Cadence tool the consumption of power and delay of the 8-bit CLA is calculated.

CLA description: Among all adder circuit CLA is one of the high speed adders by means of parallel computation simultaneously. For each addition process CLA has to detect whether the bit will generate or propagate carry bit. This will determine the carry ahead in time.

The working of CLA is based upon the generation of carry out if and only if inputs A=B=1 or when A/B = carry in = 1. Thus, defining the above condition mathematically in terms of two new signals P_i (known as carry propagate) and G_i (known as carry generate) one can write,

$$C_{i+1} = G_i + P_i C_i \qquad (1)$$
$$S_i = P_i \text{ xor } C_i \qquad (2)$$

Where, $G_i = A_i \text{ xor } B_i$ and $P_i = A_i \text{ xor } B_i$

These signals will be generated only when valid input signals are given and the output will be obtained only after one or two gate delays. So, prior calculation of carryout based on this logic rather than waiting for the previous carry to ripple through the adder to generate a new carry out reduces delay. Thus for a 4-bit CLA the four bit carry output can be estimated using the following equations,

$$C_1 = G_1 + P_1 C_0 \qquad (3)$$
$$C_2 = G_2 + P_2 G_1 + P_2 P_1 C_0 \qquad (4)$$
$$C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_0 \qquad (5)$$
$$C_4 = G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 C_0 \qquad (6)$$

Suppose that groups of 4 digits are chosen. Then the sequence of events goes something like this:
a) Each single bit adder computing the result of their own. At the same time CLA carry out its carry bit calculation.
b) The carry from LHS side started to propagate towards right side, once the carry comes in particular group within 5 gate delay.
c) The CLA unit going to reduce the carry propagation of all stages. While the first unit is going to generate a carry, the CLA capable of telling whether the next stage going to use the previous carry or miss the carry. Meanwhile the next stage CLA starts to generating its own carry.
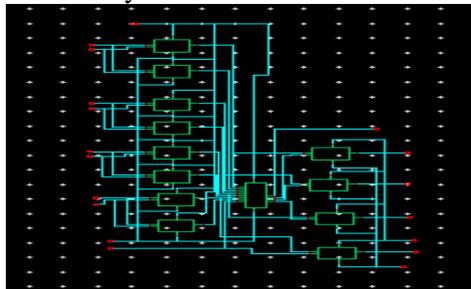

Figure.4. Schematic diagram of 4-bit CLA

The carry look ahead generator should be built for designing 4-bit CLA adder by using XOR, AND and OR gates. In order to design a 4-bit CLA, look ahead generator logic is built using the XOR, AND and OR gates. The schematic diagram for the 4-bit CLA implemented using Cadence Virtuoso tool is shown in Figure.4.

Circuit Design: The n-bit CLA is designed by using basic logic gate. The carry propagate (P_i) and carry generate (G_i) are given as inputs to the carry look ahead logic and corresponding sums and carry is obtained. The symbol representation for a 4-bit CLA is given in Figure.5.
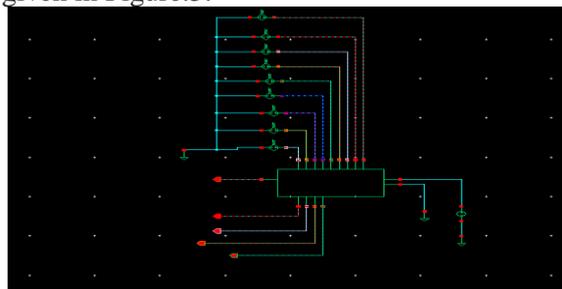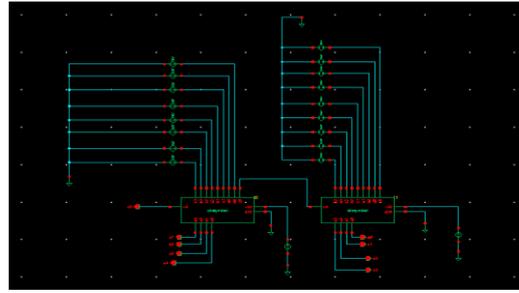

Figure.5. Symbolic representation of 4- bit CLA

Combination of two 4-bit CLA formed the 8-bit CLA. The circuit design of an 8-bit CLA is as follows Figure.6.

Figure.6. Cascaded 8-bit carry look ahead adder

Here, the input voltage given for each input is $V_{pulse} = 1V$ and the applied voltage $V_{dd}=1V$. The carry generated as output from one 4-bit CLA is given as input to another 4-bit CLA. The Boolean expressions for calculating the sum and carry outputs are given as;

$$S_n = A_n \text{ xor } B_n \text{ xor } C_{n-1} \qquad (7)$$
$$C_n = G_n + P_n.C_{n-1} \qquad (8)$$

In figure.6, the above equation is verified once after the simulation which shows the process of 8-bit CLA. From figure.6, S_n and C_n equations are verified after the simulation result. These equations ensures the operation of eight bit CLA , further analysis of 8-bit CLA has to be made for less power consumption and minimal area.

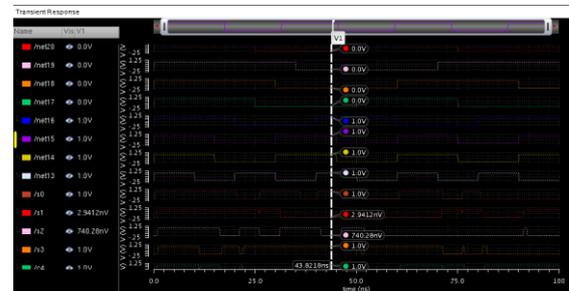**Conditions satisfied by a CLA:**

Table.1. CLA Condition

A	B	Ci	C i +1	Condition
0	0	0	0	No carry generate
0	0	1	0	
0	1	0	0	
0	1	1	1	No carry propagate
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry generate
1	1	1	1	

3. SIMULATION RESULTS AND OUTPUTS
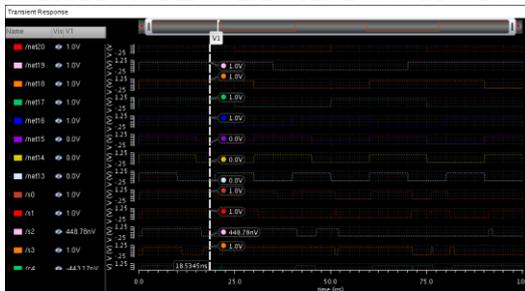
Figure.7. 4-bit CLA output waveform 1   **Figure.8. 4-bit CLA output waveform 2**

Output waveform 1: For the given inputs, the outputs are obtained as follows-

```
    Input A -     0  1  1  1
    Input B -     0  1  1  1
    C0 -                1
    ─────────────────────────
       Sum -      1  1  1  1
```

Here, there is no carry generated and hence, c4=0.

Output waveform 2:

```
    Input A -     1  0  1  1
    Input B -     1  0  1  1
    C0 -                1
    ─────────────────────────
       Sum -      0  1  1  1
```

Here, a carry is generated and hence, c4=1

Power and Delay Calculation: The power and delay calculation of eight bit CLA has been calculated for 4-bit CLA using Virtuoso tool which using 180 nm technology. Power consumption and delay calculation has been done by simulation result shown in figure.9 and figure.10.
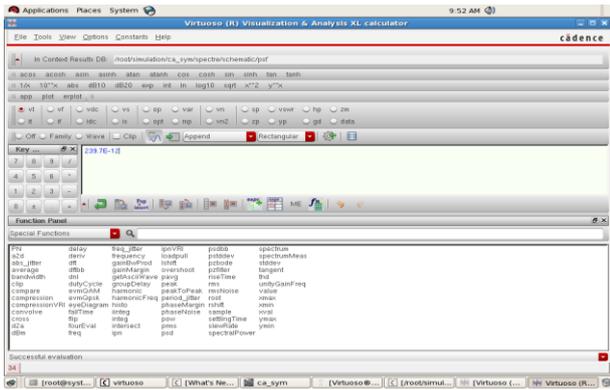
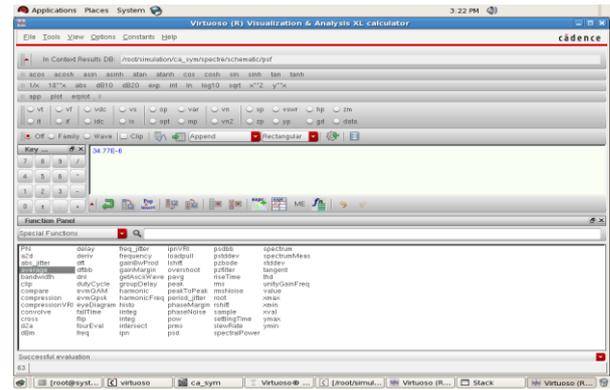|	
Figure.9. Delay computation of a 4 bit CLA	**Figure.10. 4-bit CLA power consumption report**

From the above result figure.10, it is clear that the average power consumed by the 4-bit CLA is obtained as 34.77uW and the delay is found to be 239.7ps.

Comparitive Analysis:

Table.2. Comparative analysis of 4- bit CLA

Contents	Existing System (4-Bit CLA)	Proposed System (8-Bit CLA)
Average Power (uW)	45.105 (for 4-bit CLA)	61.05
Delay (s)	$25.63*10^{-9}$	$239.6*10^{-12}$
Design type	Full adders are used	Logic gates are used

4. CONCLUSION

In Electronics, VLSI is one of the broad category. All parameter of the circuit is simulated and Evaluated through Cadence tool. Circuits parameters are simulated at supply voltage of 1V.

In this paper, 4-bit CLA consumes less power. Since 8-bit CLA is combination of two 4-bit CLA, it is also consume less power. Thus, the MCLA 8-bit carry look ahead adder have been designed with less power consumption of 61.05uW and with less delay. The results of CLA design reveal that they have acceptable performance for practical applications.

Applications:

- In digital signal processors- CLA is used to reduce the power consumptions and for battery backups in mobile phones and laptops.
- In multipliers- CLA is used to increase the speed and reduce area.
- In filtering process- the carry look ahead adder used in multipliers are used to improve its efficiency.

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